■ Tentative Specification
□ Preliminary Specification
□ Approval Specification

MODEL NO.: V500HJ1
SUFFIX: L01

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	WT Hsu

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 0.0	Sep. 2, 2011	All	All	The Tentative specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V500HJ1-L01 is a 50” TFT Liquid Crystal Display module with 12-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 16.7M colors (8-bit). The inverter module for backlight isn’t built-in.

1.2 FEATURES

- High brightness (350 nits)
- High contrast ratio (4000:1)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- RoHs compliance

1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1095.84(H) x (V) 616.41 (50” diagonal)	mm	(1)
Bezel Opening Area	1102.84(H) x 623.41(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1903(H) x 0.5708(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally Black	-	-
Surface Treatment	Anti-Glare coating (Haze 3.5%)	-	(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) Please refer sec 3.1 and 3.2 for more information of Power consumption

Note (3) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)		1142.84		mm	(1)
	Vertical (V)		663.41		mm	(1)
	Depth (D)		NA		mm	(2)
	Depth (D)		51.8		mm	(3)
Weight			12480		g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to rear.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	TST		-20	+60	ºC	(1)
Operating Ambient Temperature	TOP		0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	50	G	(3), (5)
		Z axis		35		
Vibration (Non-Operating)	VNOP		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

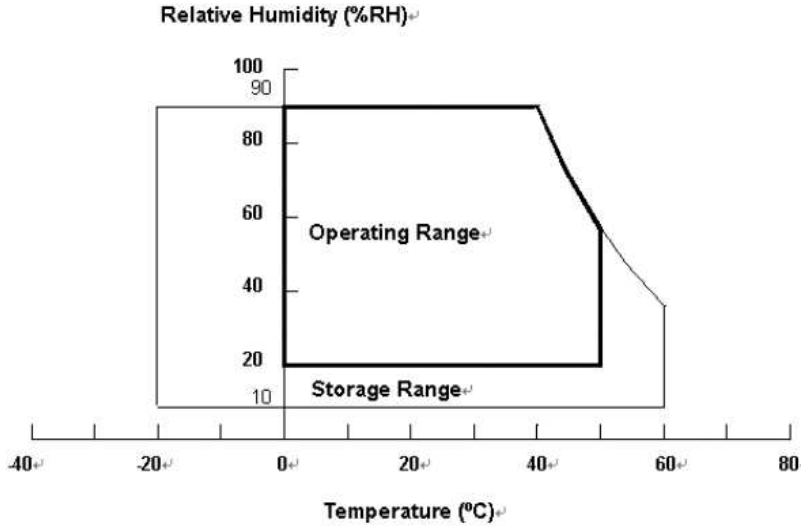
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT T-BALANCE BOARD UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	VW	–	3000	VRMS	
Input Voltage	VBL	0	170	V	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

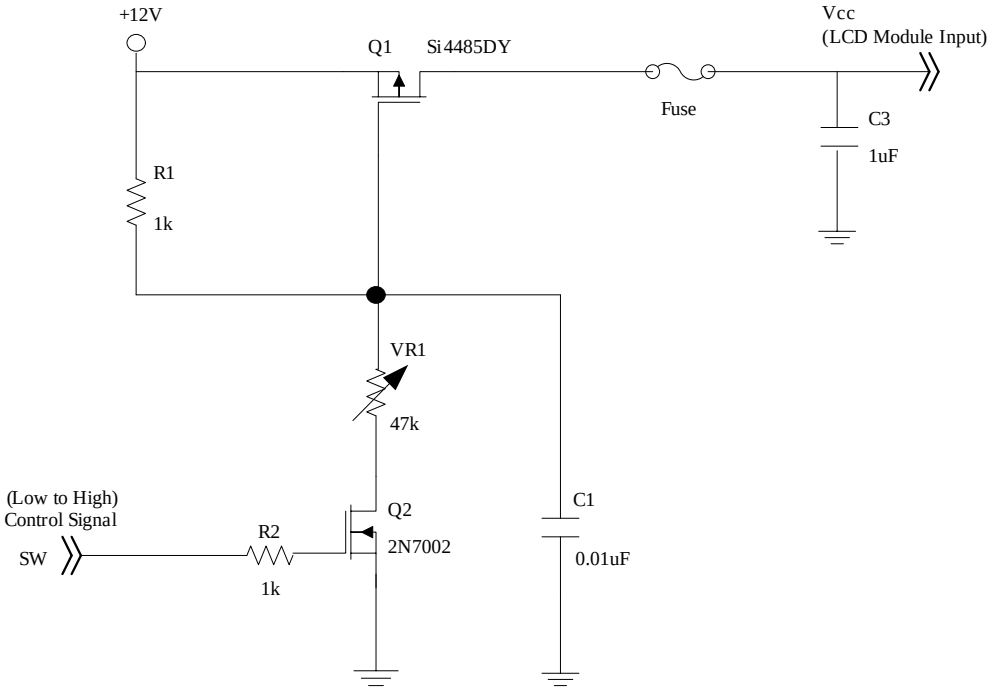
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

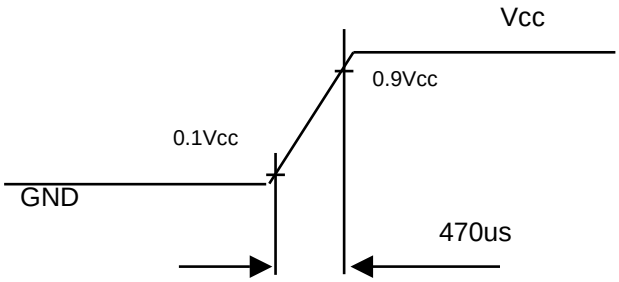
(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	(3)	A	(2)
Power consumption		P_T	—	(8.76)	(11.22)	W	(3)
Power Supply Current	White Pattern	—	—	(0.4)	—	A	(4)
	Horizontal Stripe	—	—	(0.73)	(0.85)	A	
	Black Pattern	—	—	(0.4)	—	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(5)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.



Vcc rising time is 470us



Note (3) The Specified Power consumption is under Horizontal Stripe pattern.

Note (4) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

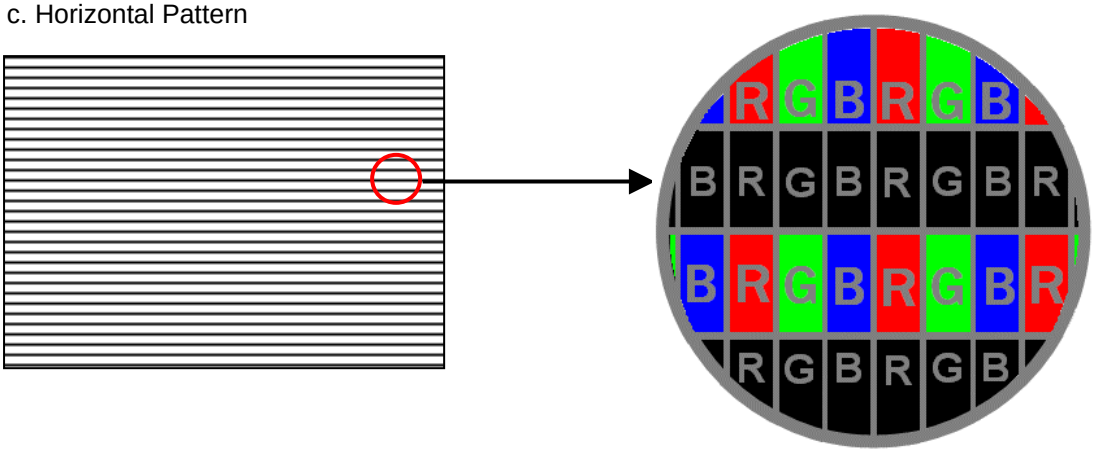
a. White Pattern

Active Area

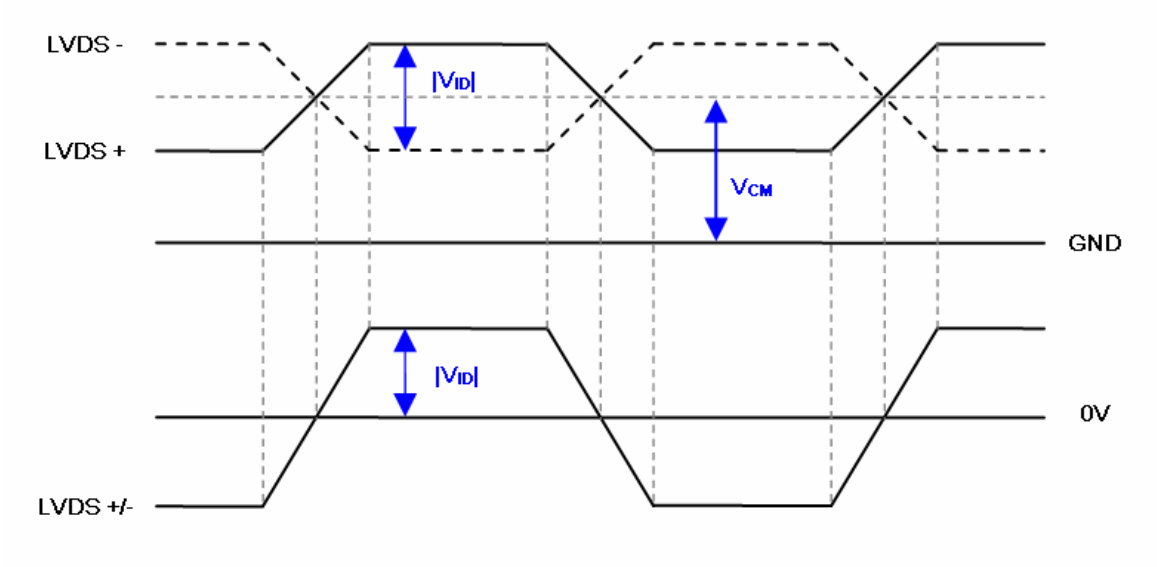
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows :



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LAMP SPECIFICATION (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_W	896	995	1095	V_{RMS}	I_L=14.5mA
Lamp Current	I_L	14	14.5	15	mA_{RMS}	
Lamp Turn On Voltage	V_S	-	1500	1900	V_{RMS}	(1) , Ta = 0 ºC
		-	1350	1650	V_{RMS}	(1) , Ta = 25 ºC
Operating Frequency	F_O	40	-	80	KHz	(2)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(3)

3.2.2 T-BALANCE BOARD INTERFACE CHARACTERISTICS

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Input Voltage		VBL+	–	(+95)	–	V	Sine Wave
Input Voltage		VBL-	–	(-95)	–	V	Sine Wave
Total Power Consumption		P_{BL}	–	(156.8)	(163.4)	W	I_L =14.5mA
Total Input Current		I_{BL}	–	(1.65)	(1.72)	A	Non Dimming
Oscillating Frequency		F_W	38	40	42	KHz	
Individual Lamp Current		I_L	14.0	14.5	15.0	mA	(3)
Protection Circuit Supply Voltage		Vcc		5	5.5	V	
Input Connector Detection	High	CNT	–	5	–	V	Normal Operation
	Low		0	–	0.8	V	Input Connector Open
Lamp Detection	High	PT	2	–	–	V	Lamp Open
	Low		–	–	1.4	V	Normal Operation
Dimming Frequency		F_B	150	160	170	Hz	
Minimum Duty Ratio		D_{MIN}	–	20	–	%	

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

Note (2) The lamp starting voltage VS should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

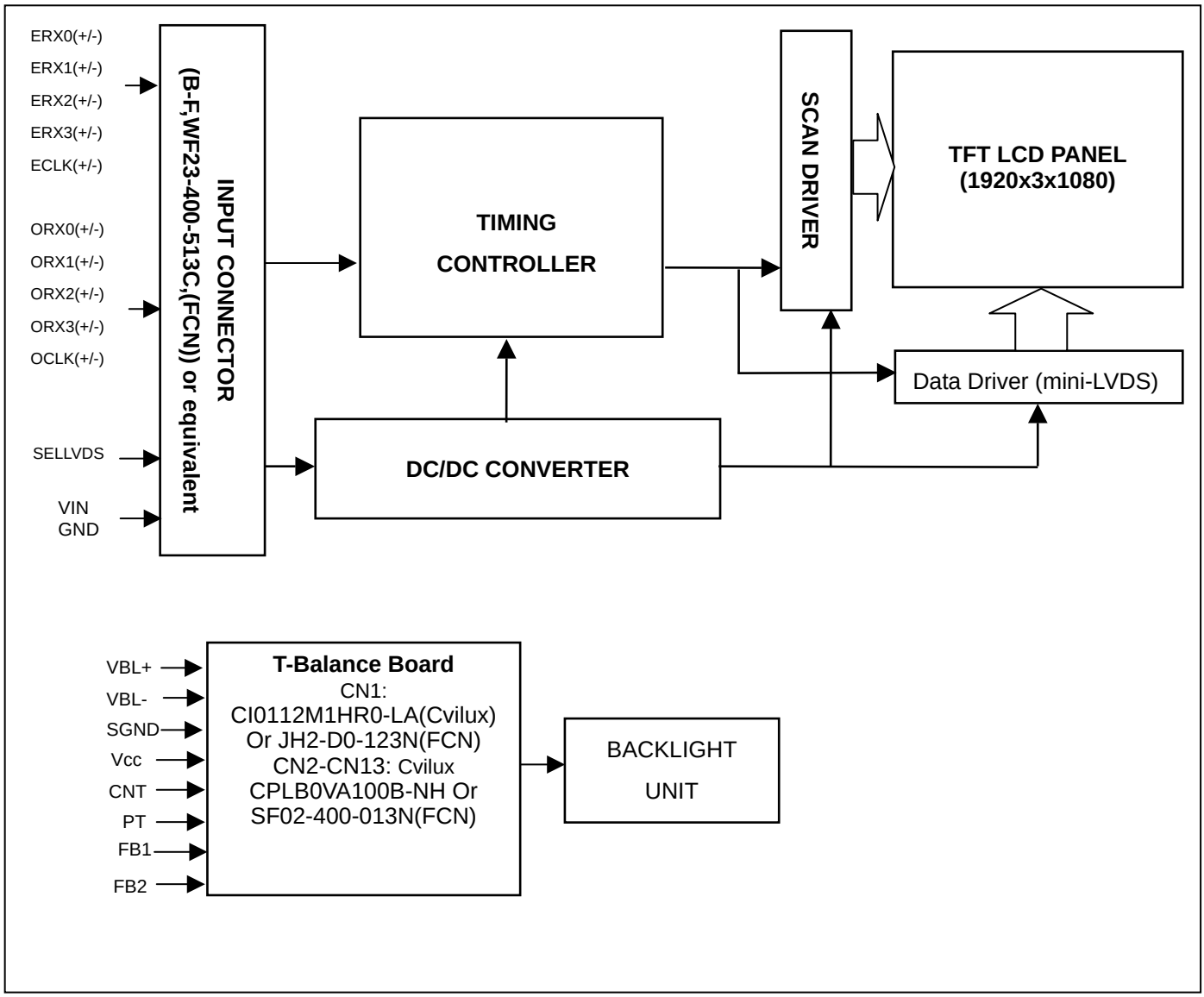
Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = (14.0~ 15.0) mArms.

Note (5) The IPI/IPB should design proper protection circuit to shut down if abnormal signals occurred of CNT/PT/FB

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



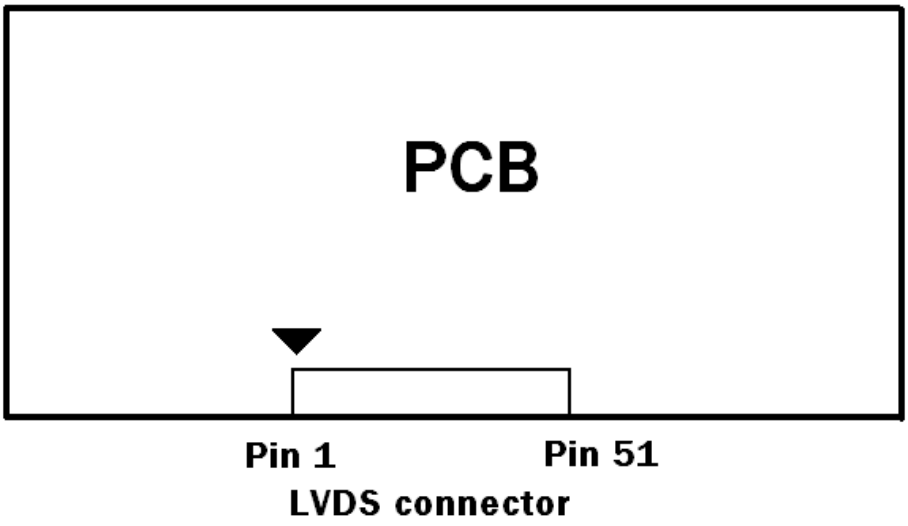
5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD INTERFACE

CNF1 Connector Part No.: B-F,WF23-400-513C,(全康-FCN) or equivalent.

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(2)
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	
7	SELLVDS	LVDS data format Selection	(3)(4)
8	N.C.	No Connection	(2)
9	N.C	No Connection	(2)
10	N.C.	No Connection	(2)
11	GND	Ground	
12	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
13	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
14	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
15	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
16	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
17	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	ECLK-	Even pixel Negative LVDS differential clock input.	(5)
20	ECLK+	Even pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
23	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(2)
25	N.C.	No Connection	
26	GND	Ground	
27	GND	Ground	
28	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
29	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
30	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
31	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
32	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
33	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	OCLK-	Odd pixel Negative LVDS differential clock input	(5)
36	OCLK+	Odd pixel Positive LVDS differential clock input	
37	GND	Ground	
38	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
39	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	(2)
41	N.C.	No Connection	
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(2)
48	VCC	Power input (+12V)	
49	VCC	Power input (+12V)	
50	VCC	Power input (+12V)	
51	VCC	Power input (+12V)	

Note (1) LVDS connector pin order defined as follows



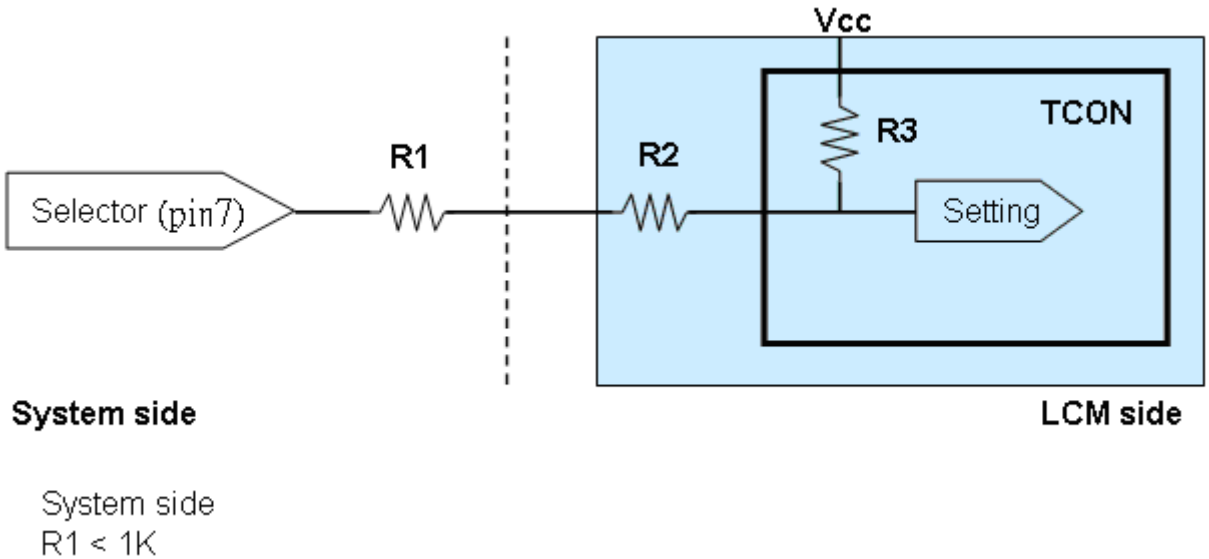
Note (2) Reserved for internal use. Please leave it open.

Note (3)

SELLVDS	Mode
L	JEIDA
H(default)	VESA

L: Connect to GND, H: Connect to Open or +3.3V

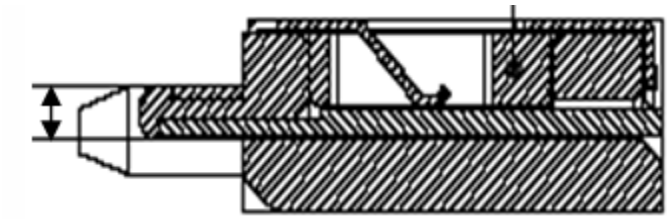
Note (4) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



System side
R1 < 1K

Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

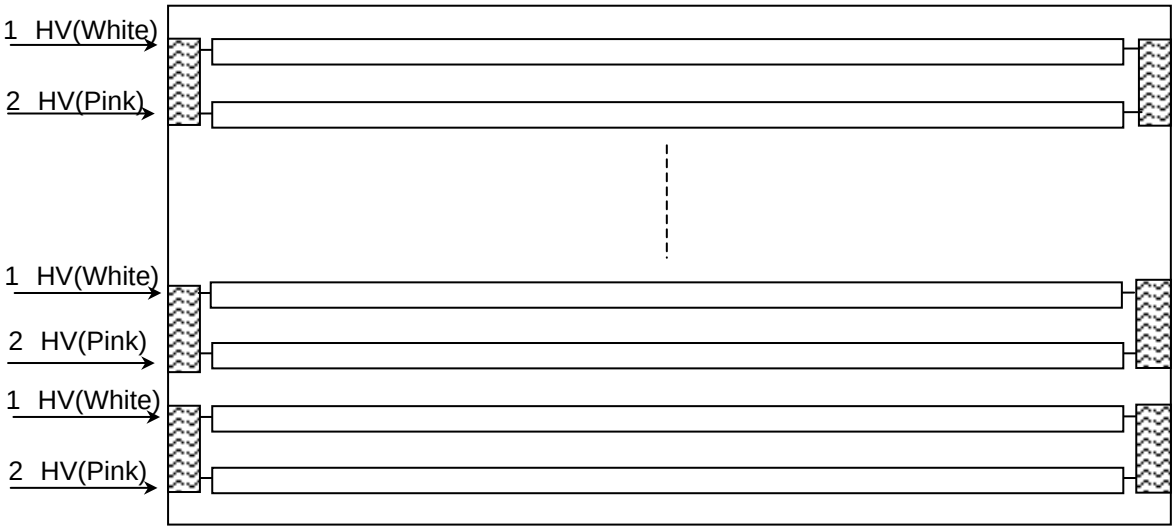
Note (6) LVDS connector mating dimension range request is 0.93mm~1.0mm as follow



5.2 BLU UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

Pin	Name	Description	Wire Color
1	HV	High Voltage	White
2	HV	High Voltage	Pink



5.3 T-BALANCE BOARD UNIT

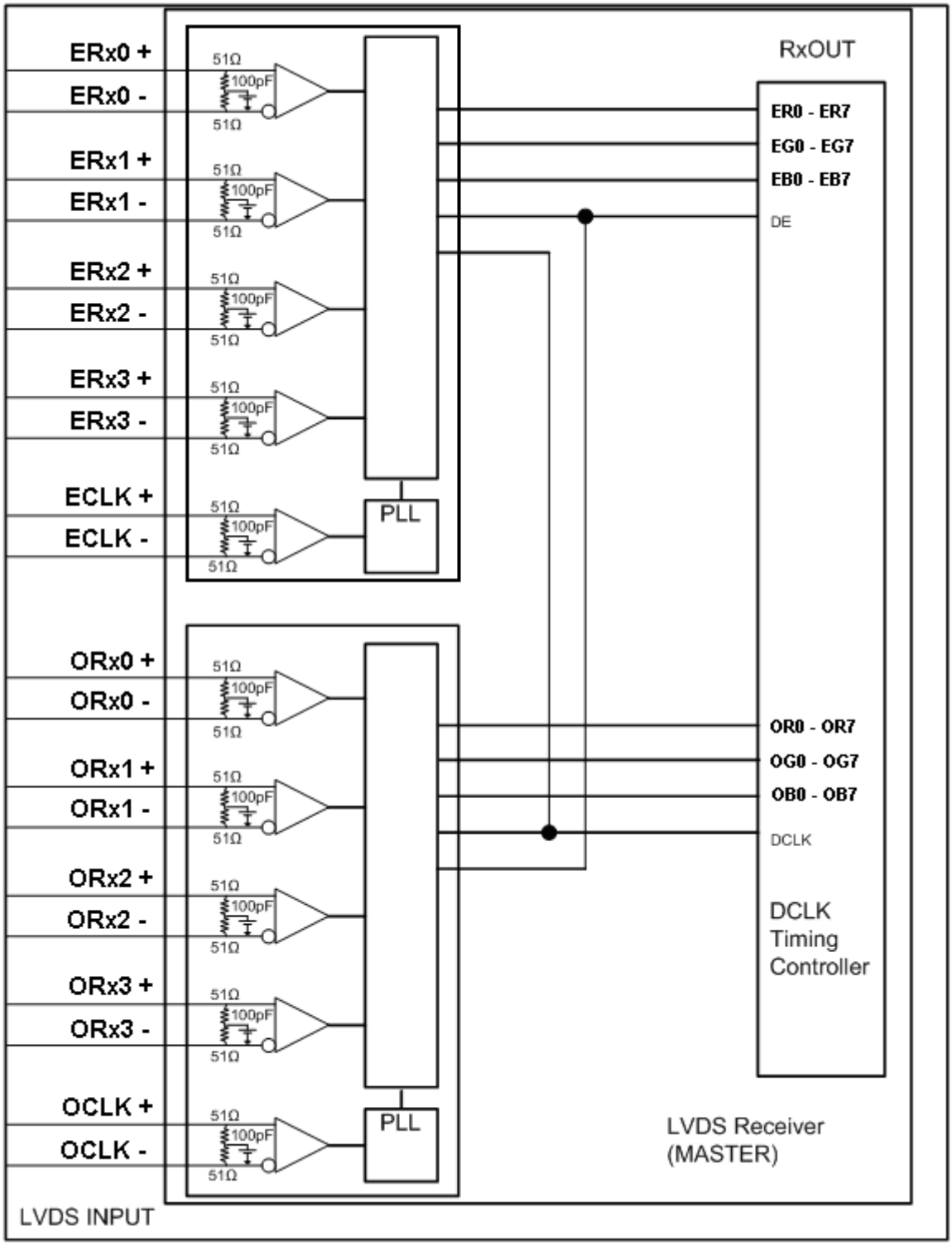
CN1: CI0112M1HR0-LA (CviLux) Or JH2-D0-123N(FCN)

Pin №	Signal name	Feature
1	VBL+	+90 V Sine Wave
2	VBL+	+90 V Sine Wave
3	N.C	No Connect
4	VBL-	-90 V Sine Wave
5	VBL-	-90 V Sine Wave
6	N.C	No Connect
7	SGND	Signal GND
8	VCC	5V
9	CNT	+5V
10	PT	+2V
11	FB1	Lamp current feedback 1
12	FB2	Lamp current feedback 2

CN2-CN13: CPLB0VA100B-NH (CviLux) SF02-400-013N(FCN)

Pin №	Signal name	Feature
1	CFL HOT	CFL High voltage

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7	Even pixel R data	OR0~OR7	Odd pixel R data
EG0~EG7	Even pixel G data	OG0~OG7	Odd pixel G data
EB0~EB7	Even pixel B data	OB0~OB7	Odd pixel B data
		DE	Data enable signal
		DCLK	Data clock signal

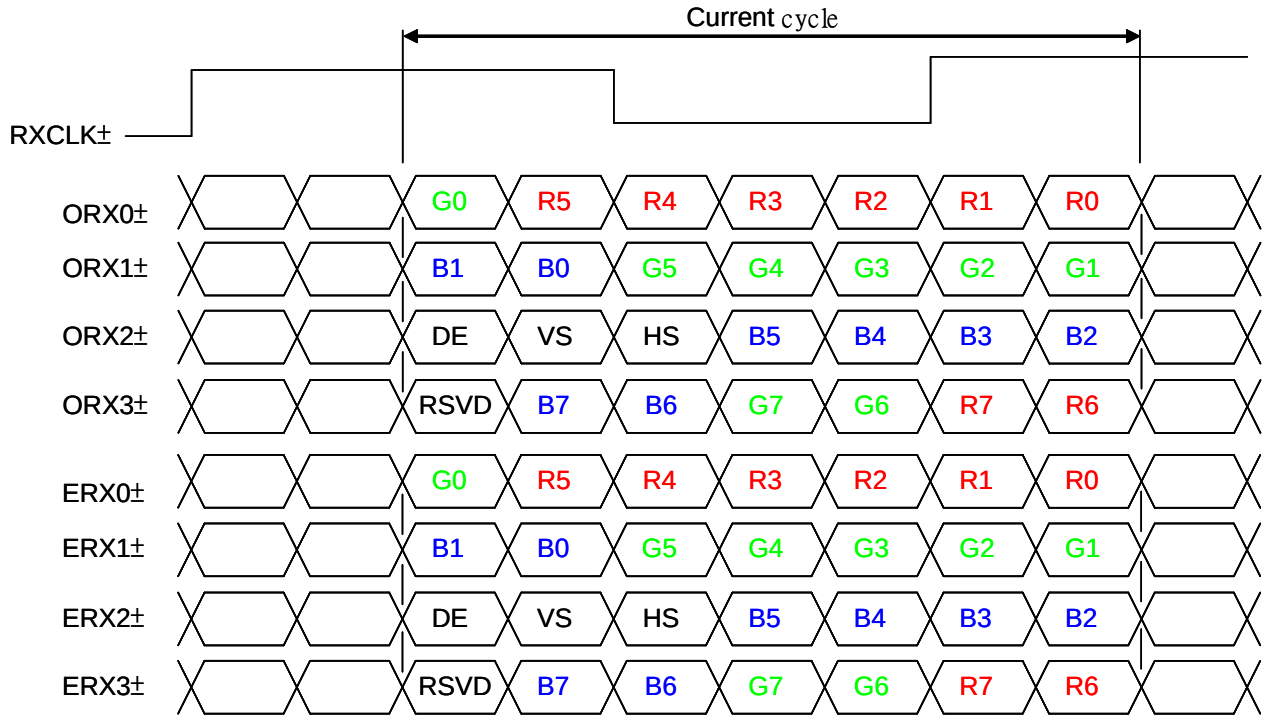
Note (1) The system must have the transmitter to drive the module.

Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

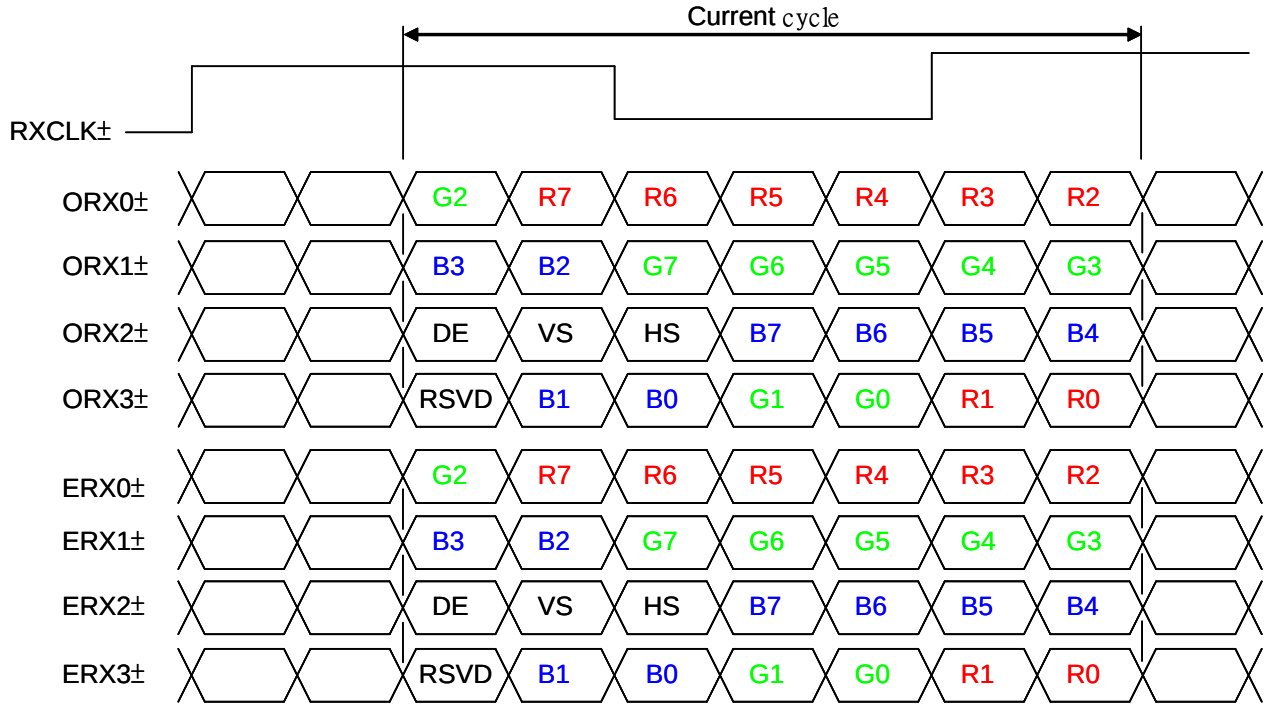
Note (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

5.5 LVDS INTERFACE

VESA Format : SELLVDS = H or Open



JEIDA Format : SELLVDS = L



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	(5)
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	(6)
		F_{r6}	57	60	63	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	
	Blank	Tvb	35	45	55	Th	
Horizontal Active Display Term	Total	Th	1050	1100	1150	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	
	Blank	Thb	90	140	190	Tc	

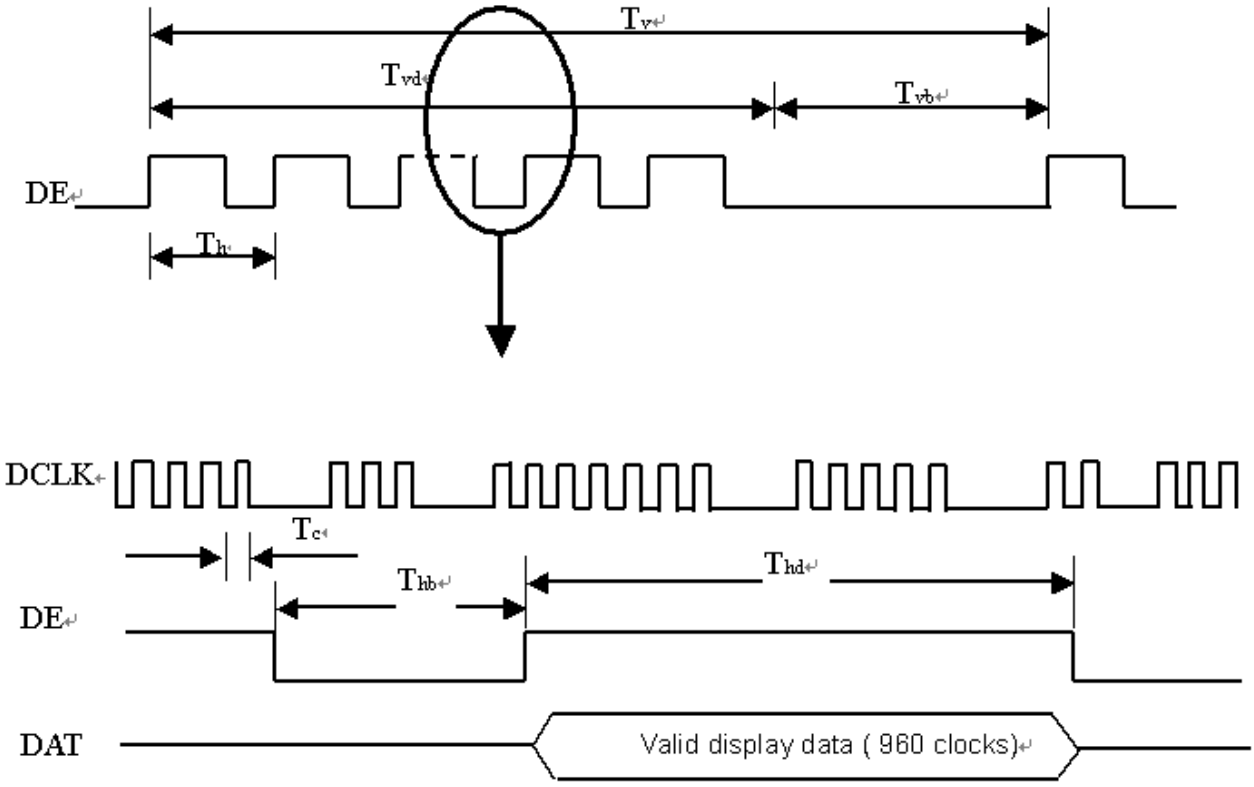
Note (1) Please make sure the range of pixel clock has follow the below equation：

$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

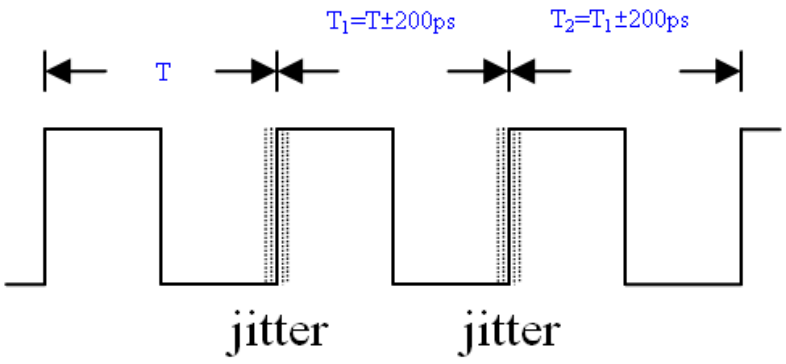
$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：

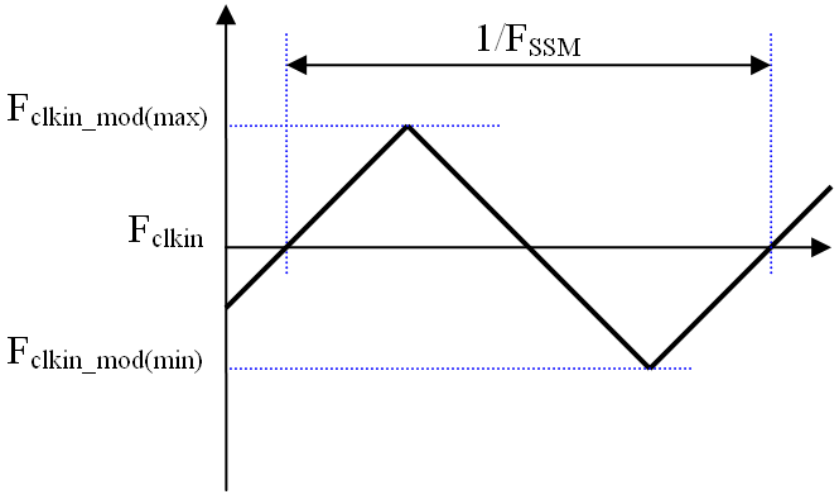
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

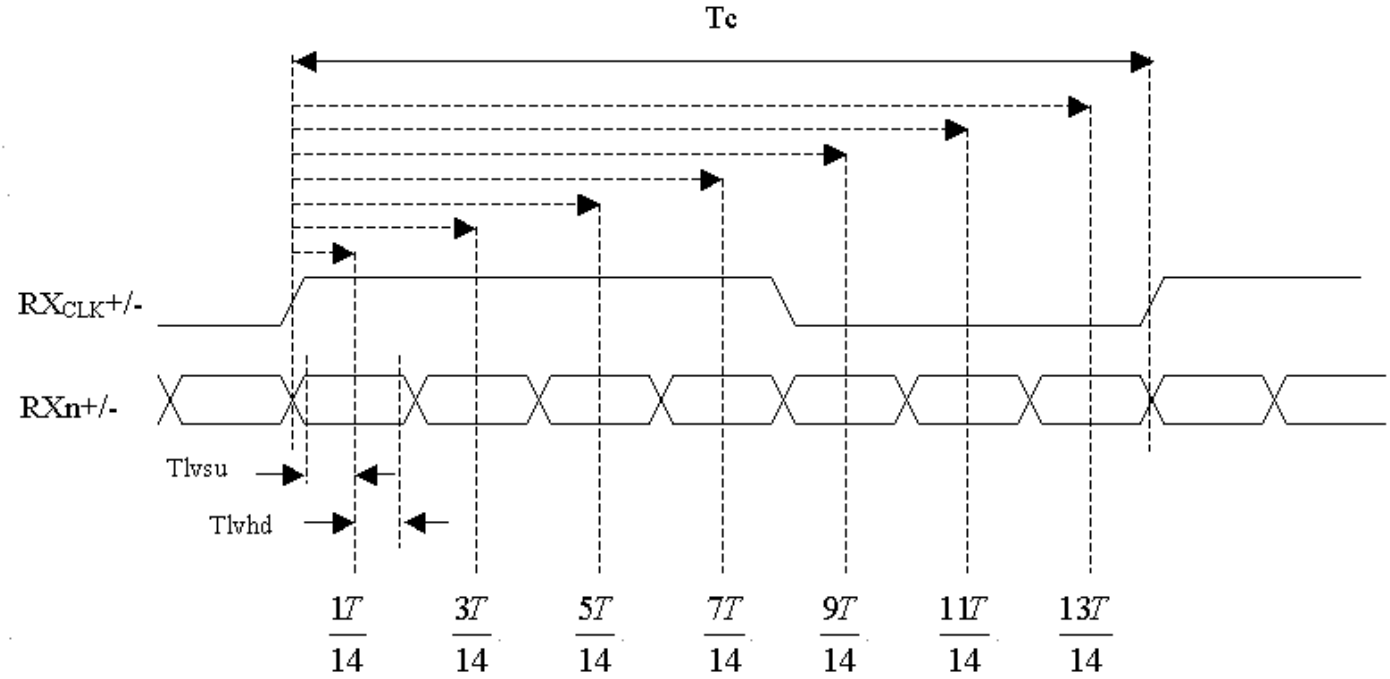


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

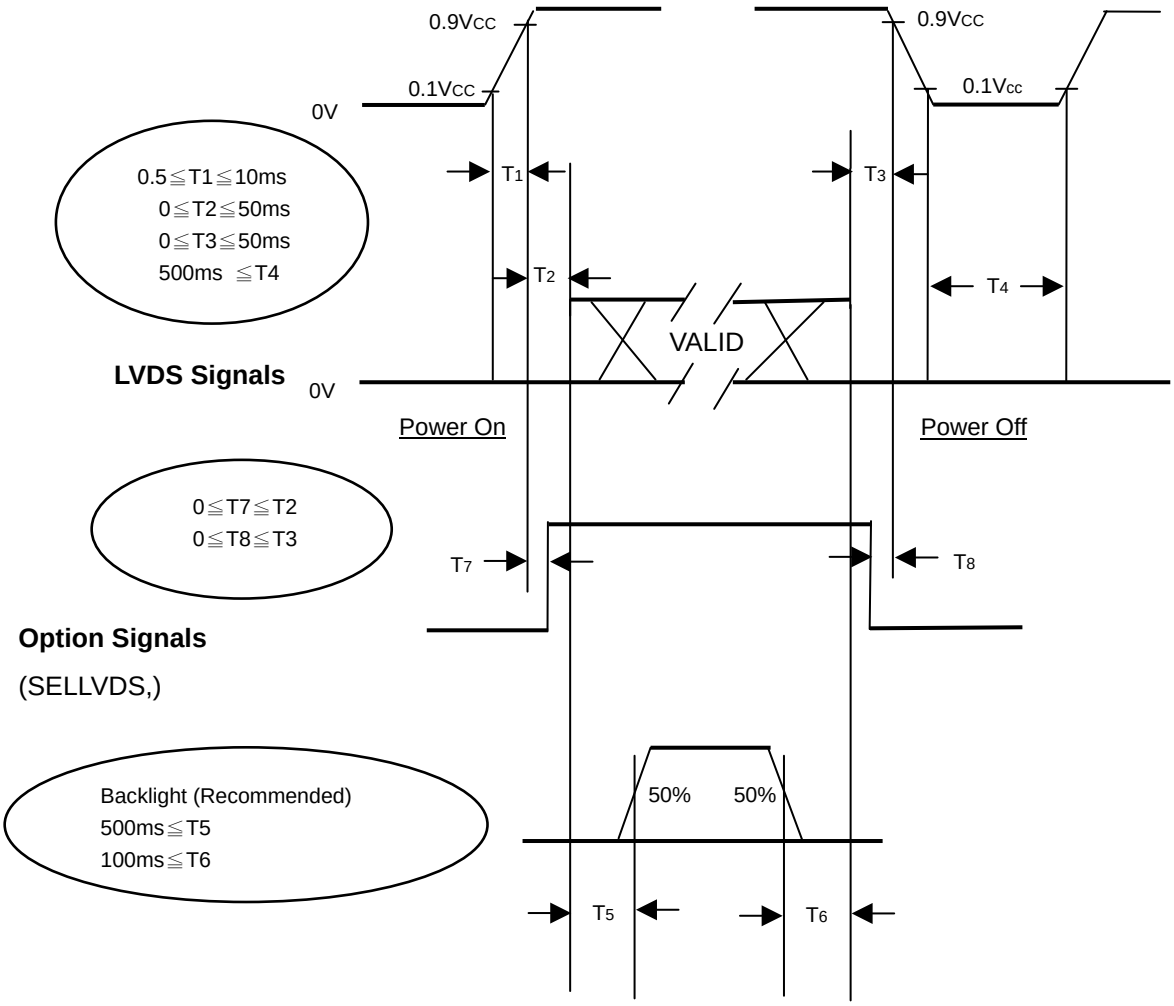
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

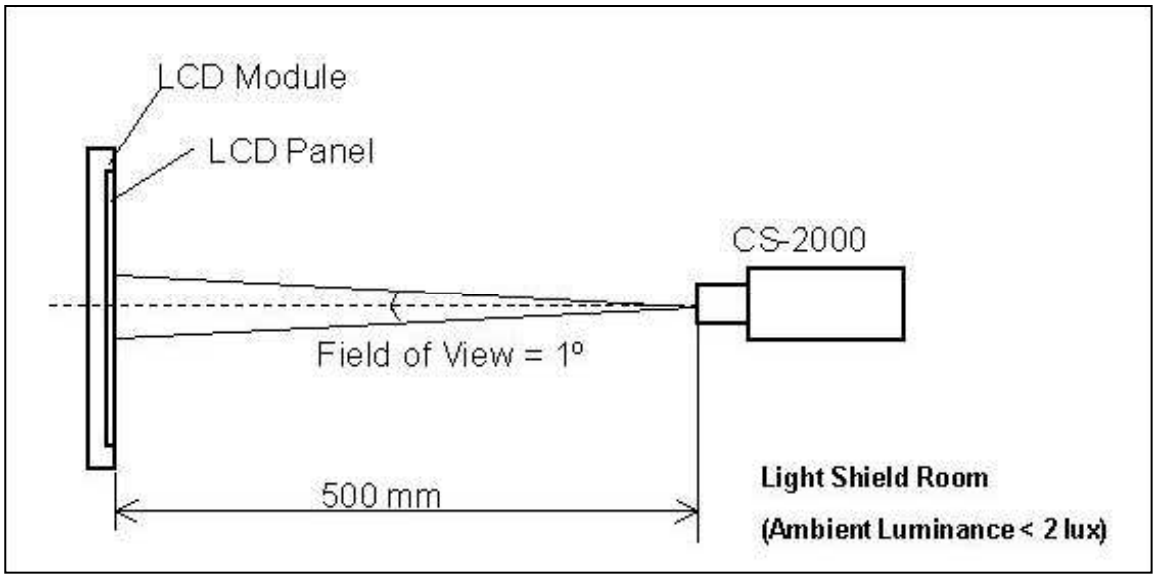
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	IL	14.5	mA
Oscillating Frequency (TBB)	FW	40	KHz
Vertical Frame Rate	Fr	60	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



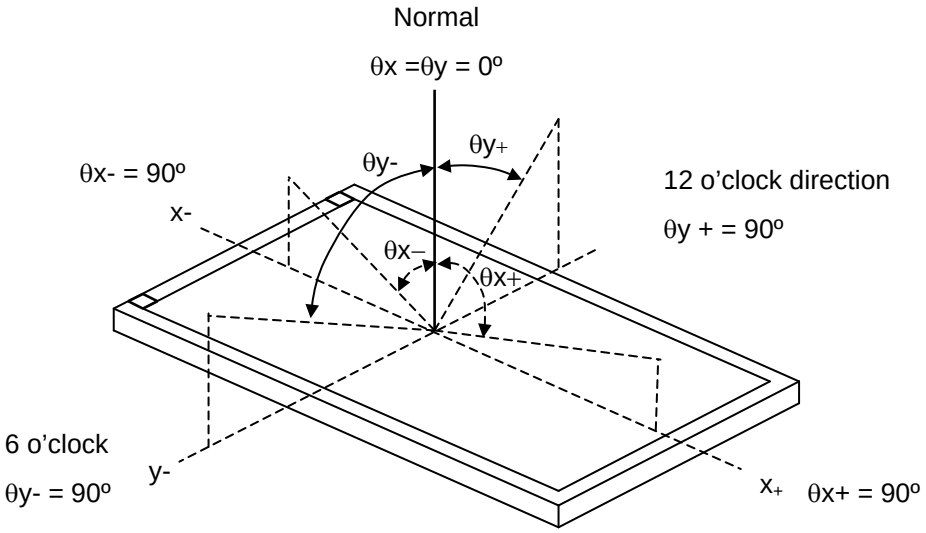
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	2800	4000	-	-	(2)
Response Time (VA)		Gray to gray		-	8	16	ms	(3)
Center Luminance of White		L_C		280	350	-	cd/m^2	(4)
White Variation		δW		-	-	1.3	-	(6)
Cross Talk		CT		-	-	4	%	(5)
Color Chromaticity	Red	Rx		Typ. -0.03	(0.628)	Typ. +0.03	-	-
		Ry			(0.321)		-	
	Green	Gx			(0.287)		-	
		Gy			(0.602)		-	
	Blue	Bx			(0.149)		-	
		By			(0.046)		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut	C.G		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	(1)
		θx-		80	88	-		
	Vertical	θY+		80	88	-		
		θY-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

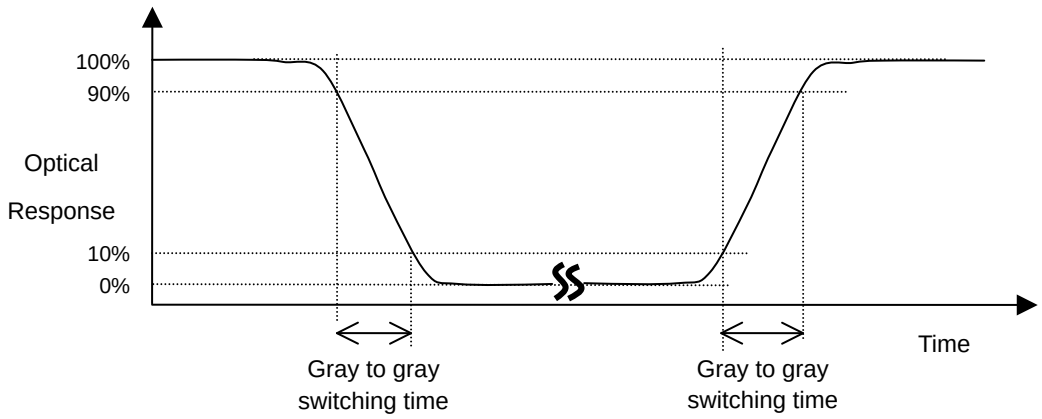
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:

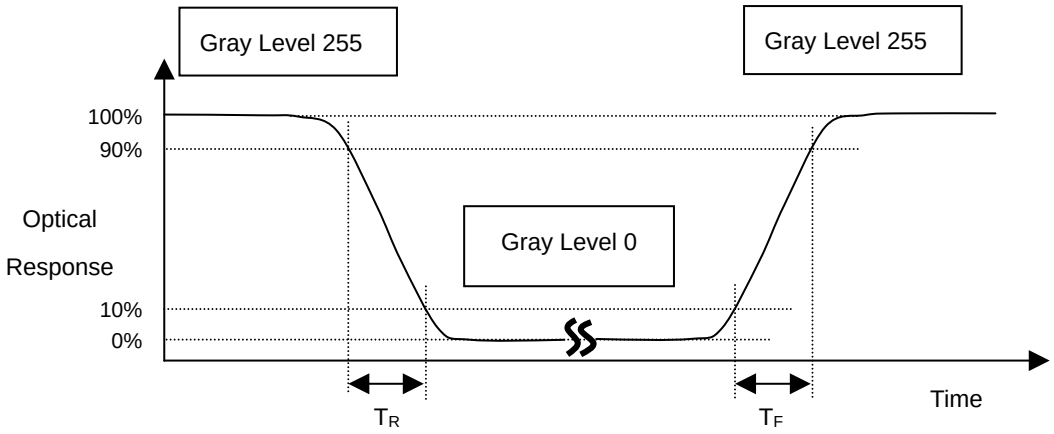


The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636,

764, 892 and 1023 to each other.

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

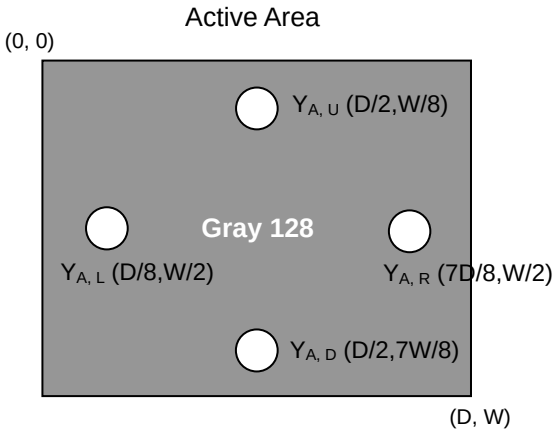
Note (5) Definition of Cross Talk (CT):

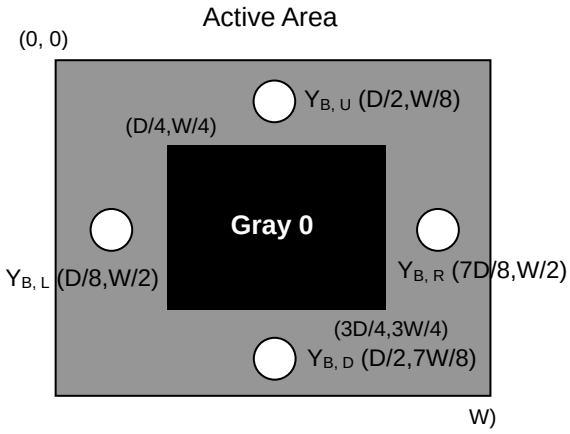
$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

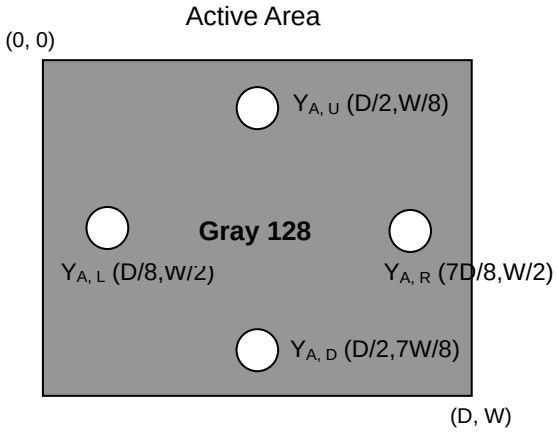
Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)

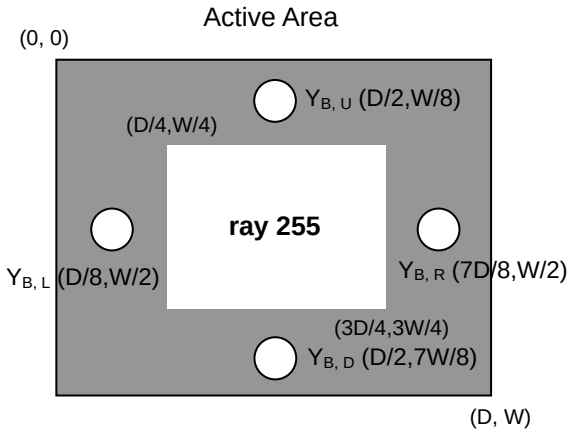




Y_A = Luminance of measured location without gray level 255 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m2)

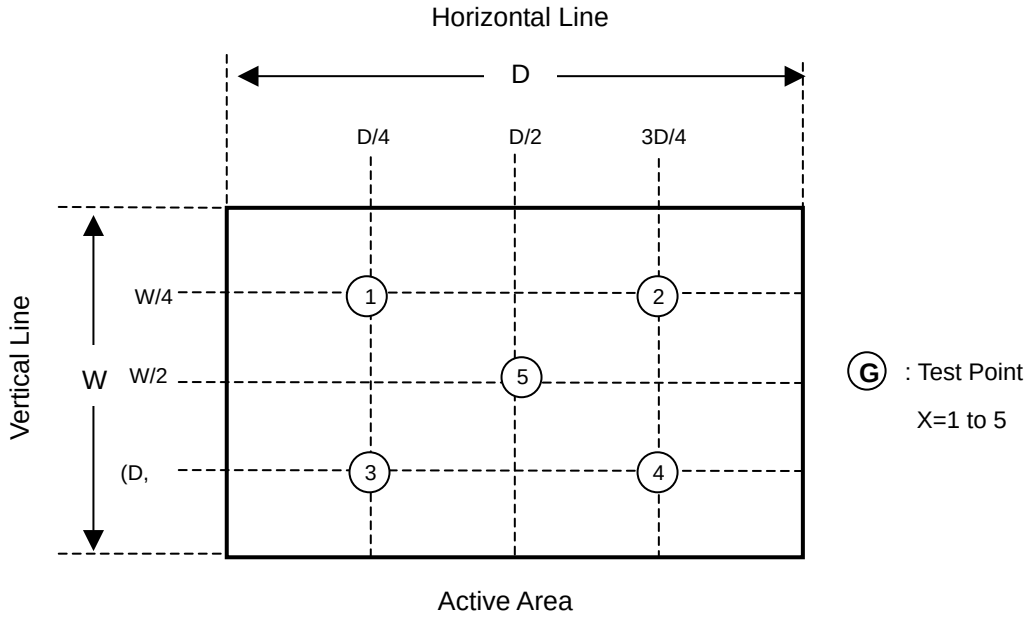




Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8 PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMIS LSI chips.

[5] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.

[6] Do not plug in or pull out the I/F connector while the module is in operation.

[7] Do not disassemble the module.

[8] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[9] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[10] When storing modules as spares for a long time, the following precaution is necessary.

[10.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[10.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[11] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

8.3 SAFETY REVIEW

8.3.1 SAFETY STANDARDS

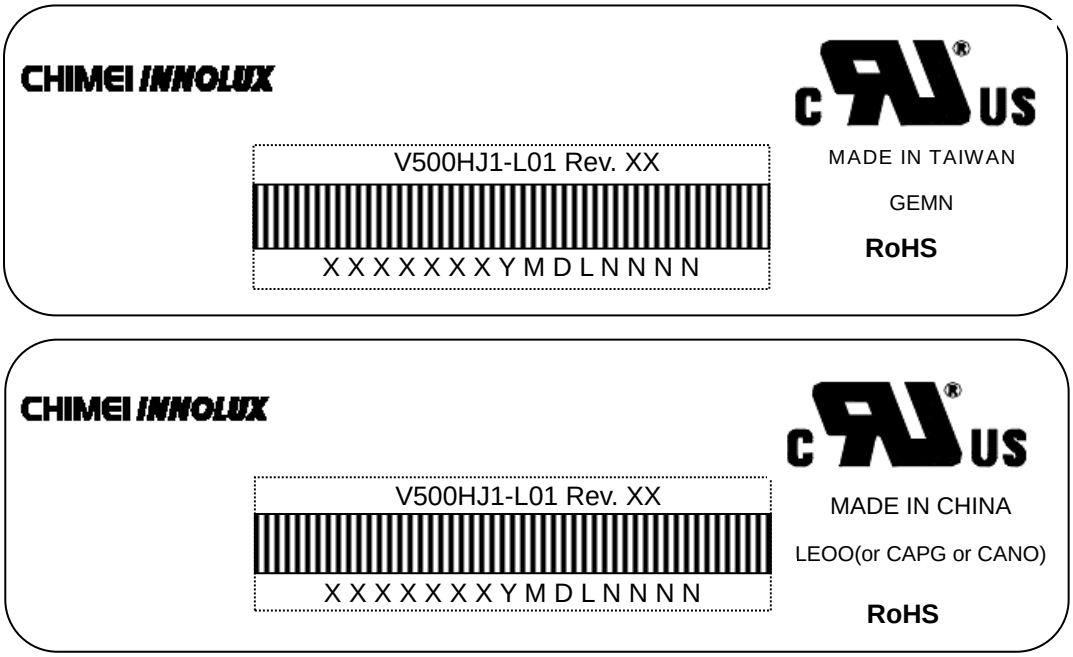
The LCD module should be certified with safety regulations as follows:

Requirement	Standard	Remark
UL	UL60950-1:2006 or Ed.2:2007	
	UL60065 Ed.7:2007	
cUL/CSA	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07	
	CAN/CSA C22.2 No.60065-03:2006 + A1:2006	
CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009	
	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006 + A11:2008	

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

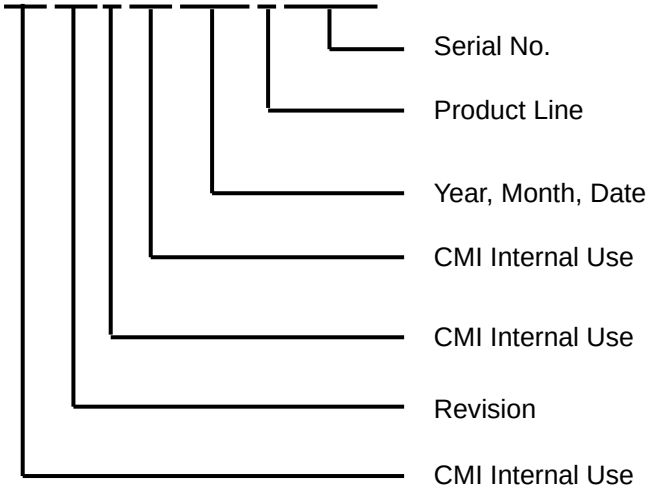
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V500HJ1-L01

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 4 LCD TV modules / 1 Box

(2) Box dimensions : 1235(L)x345(W)x751(H)mm

(3) Weight : Approx. 56.6Kg(4 modules per carton)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

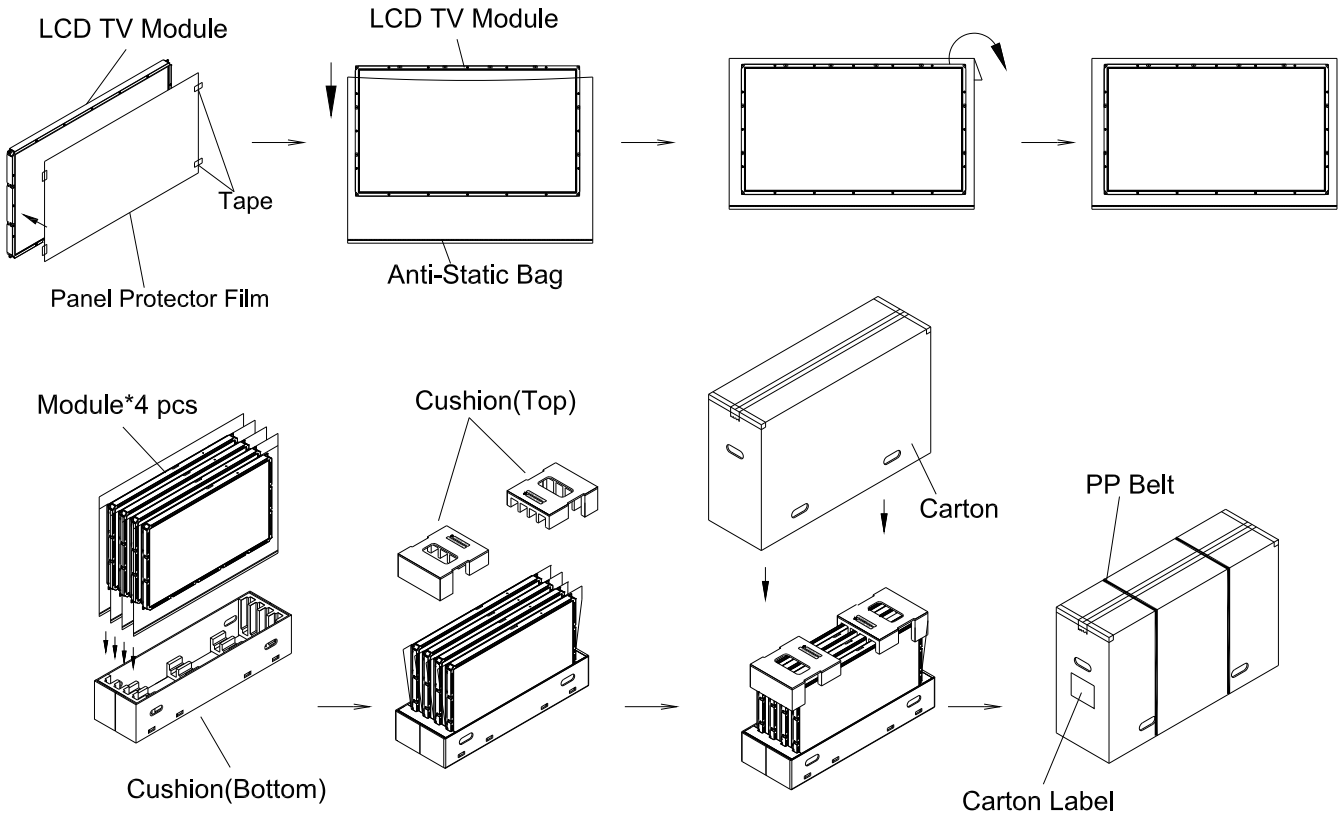


Figure 10-1 packing method

Sea / Land Transportation
(40ft HQ Container)

Sea / Land Transportation
(40ft Container)

Air Transportation

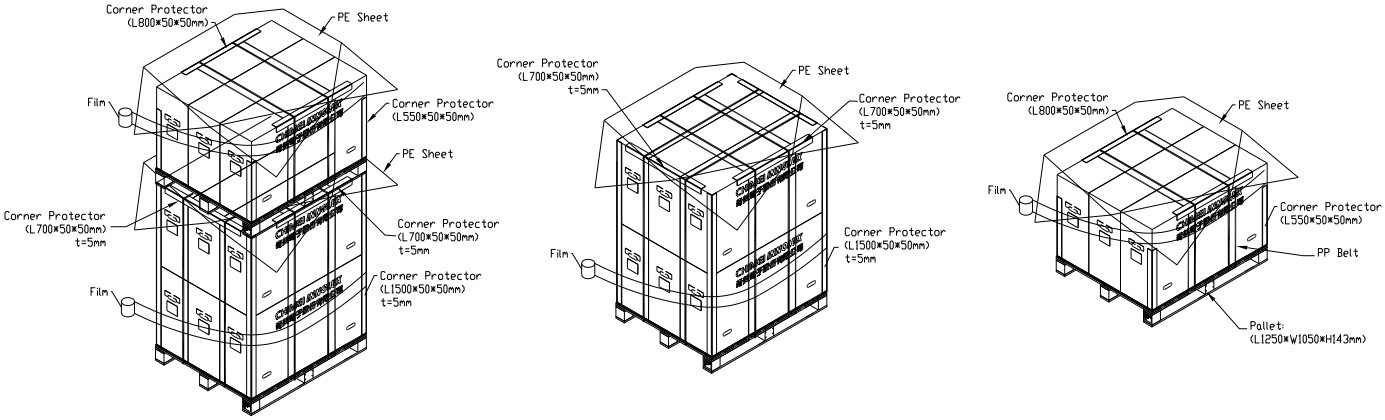


Figure 10-2 packing method

11. MECHANICAL CHARACTERISTIC